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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,436	12/12/2001	Timothy B. Cowles	00-0058.02	4282

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EXAMINER	
TU, CHRISTINE TRINH LE	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,436	COWLES ET AL.	
	Examiner	Art Unit	
	Christine T. Tu	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 58-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *58-63* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-6 have been examined.

2. Claims 58-63 have been restricted.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-6, drawn to a method of testing a memory die comprising storing a partial memory cell address on the die as a result of the testing act wherein said address corresponds to a memory cell having failed the testing act, classified in class 714, subclass 723.

II. Claims 58-63, drawn to a method for processing (a plurality of) memory circuits comprising transmitting a signal in parallel to the plurality of memory circuits and simultaneously testing the plurality of memory circuits, classified in class 714, subclass 718.

4. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case as follows:

a. invention I has separate utility such as the feature of storing a partial memory cell address which corresponds to a failed memory cell; this is a patentably distinct feature not found in invention II

b. invention II has separate utility such as the feature of transmitting a signal in parallel to the plurality of memory circuits the feature of simultaneously testing the memory circuits; this is a patentably distinct feature not found in invention I.

See MPEP § 806.05(d).

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

6. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

7. In order to expedite the prosecution for the subject application, the non-elected claims should be canceled in response to this office action.

8. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this RESTRICTION. Accordingly, **THIS RESTRICTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final restriction is set to expire ONE MONTH from the mailing date of this restriction. In the event a first reply is filed within ONE MONTH of the mailing date of this final action and the advisory action is not mailed until after the end of the ONE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than FOURTH MONTHS from the date of this final restriction.

DETAILED ACTION

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brauch et al. (6,550,023 and Brauch hereinafter) in view of Wada et al. (6,138,257 and Wada hereinafter).

12.

Claim 1:

Brauch discloses the invention substantially as claimed. Brauch teaches (figure 1) that a chip (2) comprises a memory (4), a BIST functional block (6) and bitmap storage (18). The BIST functional block (6) is firmware that controls the execution of on-chip memory tests to detect and locate defects in the memory (4). When a corrupt cell is detected, the bitmap storage (18) stores comparison mismatch information comprising a complete bitmap of the precise location of failed cells in the memory (4) (figure 1, column 3 lines 15-48).

Brauch does not explicitly teach that a chip is placed a location outside of a production facility. Wada, however, teaches that in some cases, defect analysis test is performed off the mass production line extractively for selected ones of ICs (column 2 lines 41-45). It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Brauch's chip would have been performing the memory test when the chip is off the mass production line (as suggested by Wada).

One having ordinary skill in the art would be motivated to do so because Wada teaches that selected ones of ICs can be tested off the mass production line (column 2 lines 40-45).

Claims 2-6

Brauch's memory (4) is part of a chip (2) that can be an electronic system, a computer system or a telephone system.

Response to Arguments

13. Applicant's arguments filed October 20, 2005 have been fully considered but they are not persuasive.

For claim 1, applicants argue that Wada does not teach or suggest the limitation of "allowing a memory die to be placed in a location outside of a production facility of the die". With Wada's teaching "In some case, ... defect analysis test is performed **off** the mass production line extractively for selected ones of the manufactured ICs rather than an the mass production line for every manufactured IC... " (column 2 lines 41-44), applicants argue that Wada teaches away the claimed invention.

Examiner, however, respectfully traverses applicants' remarks. Due to the breath of the claim, "allowing a memory die to be placed in a location outside of a **production facility** of the die" is recited. It is the examiner's position that the claimed "production facility" would have been Wada's manufacture line since there is no specific

type of production facility is being recited. Therefore, Wada's "defect analysis test is performed **off** the mass production line ... for selected ones manufactured of ICs" (column 2 lines 41-43) is equivalent to applicant's "testing said memory die while said die is in said location (**outside** of a production facility of said die)".

Applicants further argue that Wada's extractive defect analysis test is not desirable and would present the problem that a longer test time is required. Such test desire and such time **are not recited** in the claim. In addition, applicant should also note that the claim 1 is recited with the transitional term "comprising" (at line 1 of claim 1) which inclusive or open-ended and does not exclude additional un-recited elements or means.

For claims 58-63, these claims have been restricted. Therefore, they have not been examined (see Restriction ¶s 3-9 above).

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christine T. Tu
Primary Examiner
Art Unit 2138

January 11, 2006